signals to a gate of said first switching MOS transistor and a gate of said second switching MOS transistor, respectively, so that operation of said pair of N-channel MOS transistors is started at a time different from the time when operation of said pair of P-channel MOS transistors is started.

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~~25~~. A semiconductor memory according to claim ~~23~~ 4, further comprising a fourth switching MOS transistor of N-channel type having a drain coupled to said source of each of said pair of N-channel MOS transistors and a source coupled to said first potential terminal, wherein said fourth switching MOS transistor is turned "on" at a time different from the time when said first switching MOS transistor is turned "on". --

REMARKS

Entry of this Amendment prior to examination is respectfully requested. By the present Amendment, new claims 20-25 are presented for examination, noting that these claims are directed to particular features of an amplifier and precharging circuit for operation in conjunction with a plurality of dynamic memory cells.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account